

Amendments to the Claims

 Please amend the claims as follows:


Claims 1-32 (canceled).

33. **(currently amended)** A method of fabricating a plurality of individual chips for conducting chemical reactions, said method comprising:

(a) preparing a plurality of said chips on a single silicon substrate, wherein each of said chips comprises an array ~~has a matrix~~ of electronically addressable sites, each site for electronically carrying out a chemical reaction and each site comprising an electrode, and

(b) severing said single silicon substrate into said individual chips wherein each of said chips comprises an array of electronically addressable sites and each site comprising an electrode.

34. **(currently amended)** A method of fabricating a plurality of individual chips for conducting a part of a synthesis of oligonucleotides, said method comprising:

 (a) preparing a plurality of said chips on a single silicon substrate, wherein each of said chips comprises an array ~~has a matrix~~ of electronically addressable sites, each site for electronically carrying out a part of a synthesis of oligonucleotides and each site comprising an electronic cell within said silicon substrate, and

(b) severing said single silicon substrate into said individual chips wherein each of said chips comprises an array of electronically addressable sites and wherein each of said sites comprises an electronic cell within said silicon substrate.

35. **(currently amended)** A method of fabricating a plurality of individual chips for conducting a synthesis of oligonucleotides to form oligonucleotide arrays, said method comprising:

(a) preparing a plurality of said chips on a single silicon substrate, wherein each of said chips comprises an array ~~has a matrix~~ of electronically addressable sites, each site for electronically carrying out a synthesis of an oligonucleotide of said oligonucleotides to form oligonucleotide arrays, and

(b) severing said single silicon substrate into said individual chips wherein each of said chips comprises an array of electronically addressable sites and wherein each of said sites comprises an electrode within said silicon substrate.